IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Lukanc et al.
Serial No.:	10/790,590
Filed:	March 1, 2004
Group Art Unit:	2825
Before the Examiner:	Whitmore, Stacy
Title:	SYSTEM AND METHOD FOR DESIGNING AN INTEGRATED CIRCUIT DEVICE

REPLY BRIEF UNDER 37 C.F.R. §41.41

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is being submitted in response to the Examiner's Answer dated May 18, 2007, with a two-month statutory period for response set to expire on July 18, 2007.

I. RESPONSE TO EXAMINER'S ARGUMENTS:

A. Response to Examiner's assertion that the Examiner has provided appropriate motivation for modifying White with Hatsch to include the missing claim limitation of claims 1 and 31, as discussed on pages 10-12 of Examiner's Answer.

The Examiner states that White discloses physical verification of an electronic design. Examiner's Answer, page 11. The Examiner further states that Hatsch is concerned with the design and verification of the circuit design. *Id.* The Examiner cites column 2, line 59 – column 3, line 16 as well as column 14, lines 20-40 of Hatsch in support of the statement. *Id.* Hatsch teaches using a simulator to check the functional capability. Column 2, lines 59-60. Hatsch further teaches that one predetermined optimization parameter used in optimizing the layout of the cells of an integrated circuit may be switching speed of an integrated circuit. Column 14, lines 18-37. The Examiner then concludes that it would be obvious to modify White to include the aspect of having the desired electrical characteristics include at least one of gain and switching speed, as recited in claim 1 and similarly in claim 31, "in order to design a circuit with performance being the objective." Examiner's Answer, page 11. The Examiner's motivation is insufficient to establish a *prima facie* case of obviousness in rejecting claims 1-4, 6-20 and 31.

The Examiner appears to mainly focus on the fact that both White and Hatsch are concerned with verifying the design of a circuit design as support for the Examiner's motivation. This alone does not provide motivation for modifying White with Hatsch. There are thousands of patents and articles that are concerned with verifying the design of a circuit design. Why not combine White with any one of those patents?

Further, while Hatsch does teach using switching speed as a predetermined optimization parameter used in optimizing the layout of the cells of an integrated circuit, where is the motivation for modifying White to include the aspect of switching speed? In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same

problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner has not provided reasons as to why White would use switching speed except the fact that another reference teaches switching speed. Simply because the references can be combined or modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. §2143.01. Hence, the Examiner's stated motivation is insufficient to support a *prima facie* case of obviousness in rejecting claims 1-4, 6-20 and 31. *Id.*

Further, the Examiner appears to state a new motivation ("in order to design a circuit with performance being the objective") in connection with modifying White to include the aspect of using switching speed as a desired electrical characteristic. Examiner's Answer, page 11. The Examiner had previously stated "optimizing layouts for functional capability and desired requirements concerning critical paths would improve design and circuit performance" as motivation for modifying White to include the aspect of using switching speed as a desired electrical characteristic. Office Action (10/23/2006), page 6. Concerning the newly stated motivation, how does this provide a reason for modifying White to include the aspect of using switching speed as a desired electrical characteristic? There are many ways in designing a circuit with performance being the objective. Why in particular would White use switching speed?

Hence, the Examiner's motivation does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify White to include the missing claim limitation of claims 1 and 31. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-4, 6-20 and 31. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

With respect to the Examiner's comment on page 12 concerning removing the limitation of drive current from the respective claims, Appellants only removed the limitation of drive current from the respective claims to broaden the scope of the claims. Appellants did not remove the limitation of drive current from the respective claims in response to the Examiner's cited passage in White.

B. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table" as recited in claim 3, as discussed on page 12 of Examiner's Answer.

The Examiner appears to assert that feature dimension variation 644 of White teaches actual electrical characteristics associated with the actual dimensions of the structures. Examiner's Answer, page 12. Appellants respectfully traverse. There is no language in the cited passage (paragraph [0211] of White) that teaches that feature dimension variation 644 corresponds to electrical characteristics or corresponds to actual electrical characteristics or corresponds to actual electrical characteristics associated with the actual dimensions of the structures. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 3, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

C. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input" as recited in claim 4, as discussed on page 13 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraph [0285] and Figure 53 of White as teaching "wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input" as recited in claim 4. Examiner's Answer, page 13. Appellants respectfully traverse.

White instead teaches that the third framework, Figure 53, is an extension of the client-server model that includes communication via a network 2376 with additional computers that may contain one or more components of the system described in sections b. through f. [0285].

There is no language in the cited passages that teaches determining actual electrical characteristics. Neither is there any language in the cited passages that teaches that the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 4, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

D. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation" as recited in claim 6, as discussed on page 13 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraphs [0006-0008, 0118 and 0137] of White as teaching "wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation" as recited in claim 6. Examiner's Answer, page 13. Appellants respectfully traverse.

White instead teaches that generating includes using optical proximity correction to adjust the design for optical interference effects. [0006]. White further teaches that a computer-aided-design system 36 is used to translate a functional circuit design to an electronic layout design file that represents a physical device, layer-by-layer. [0118]. White additionally teaches that an IC design is commonly represented electronically in a library of files that define structures and their locations at each level of an integrated circuit 280. [0137].

There is no language in the cited passage that teaches that the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 6, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

E. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design" as recited in claim 7, as discussed on page 14 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraphs [0006, 0118, 0140 and 0141] of White as teaching "wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design" as recited in claim 7. Examiner's Answer, page 14. Appellants respectfully traverse.

White instead teaches that generating includes using optical proximity correction to adjust the design for optical interference effects. [0006]. White further teaches that a computer-aided-design system 36 is used to translate a functional circuit design to an electronic layout design file that represents a physical device, layer-by-layer. [0118]. White further teaches that one option to use models in which the lithography process flow 600 is defined to include not only the lithography process step but may also include pre and post photoresist deposition and subsequent plasma etch. [0140]. Additionally, White teaches that the predicted feature dimension variation 680 and the desired feature dimension specification and tolerances 750 are input into a verification and correction component 800 which identifies any features that will exceed or approach the tolerances. [0141].

There is no language in the cited passages that teaches that the initial IC device design includes a desired relationship between at least two structures within the IC device design. Therefore, the Examiner has not presented a *prima facie* case of

obviousness in rejecting claim 7, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

F. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design" as recited in claim 8, as discussed on page 14 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraphs [0135, 0137-0138 and 0140] of White as teaching "determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design" as recited in claim 8. Examiner's Answer, page 15. Appellants respectfully traverse.

White instead teaches that IC pattern dependent relationships can be used to verify whether feature dimensions produced by lithography match the dimensions as they were designed, and, if not, to modify the design layout and masks to yield the designed features. [0135]. White further teaches that the variation of the resulting fabricated device can be measured physically, such as by optical measurement of the film thickness or surface profiling of the wafer surface to determine actual topography. [0138]. White additionally teaches that one option to use models in which the lithography process flow 600 is defined to include not only the lithography process step but may also include pre and post photoresist deposition and subsequent plasma etch. [0140].

There is no language in the cited passages that teaches determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 8, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

G. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity" as recited in claim 12, as discussed on page 15 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraph [0138] of White as teaching "measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity" as recited in claim 12. Examiner's Answer, page 15. Appellants respectfully traverse.

White instead teaches that the variation of the resulting fabricated device can be measured physically, such as by optical measurement of the film thickness or surface profiling of the wafer surface to determine actual topography. [0138].

There is no language in the cited passage that teaches measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 12, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

H. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 14, as discussed on pages 15-16 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraphs [0112-0115, 0133 and 0138] of White as teaching "wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation

will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 14. Examiner's Answer, page 16. Appellants respectfully traverse.

White instead teaches that lithography is a frequently repeated process step during the manufacture of ICs in which a pattern that defines the dimensions of the circuitry is transferred to a silicon wafer. [0115]. White further teaches that the patterns are subsequently used with the etch process to physically etch the features into the wafer surface or other thin films deposited on the wafer surface. [0115]. White additionally teaches that process related pattern-dependencies may also occur within the lithography process itself where the density of features often affect how well the printed features reproduce those designed. [0133]. Furthermore, White teaches that layout features 280 of the design are mapped 310 to parameters of wafer topography 580, such as film thickness, dishing, erosion, and total copper loss. [0138].

There is no language in the cited passages that teaches simulating how structures within the layout representation will pattern as a function of the size of a structure with respect to other adjacent structures. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 14, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

I. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, and (ii) (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 17, as discussed on pages 16-17 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraphs [0112-0115, 0133 and 0139-0144] of White as teaching "wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, and (ii) (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 17. Examiner's Answer, page 17. Appellants respectfully traverse.

White instead teaches that lithography is a frequently repeated process step during the manufacture of ICs in which a pattern that defines the dimensions of the circuitry is transferred to a silicon wafer. [0115]. White further teaches that the patterns are subsequently used with the etch process to physically etch the features into the wafer surface or other thin films deposited on the wafer surface. [0115]. White additionally teaches that process related pattern-dependencies may also occur within the lithography process itself where the density of features often affect how well the printed features reproduce those designed. [0133]. Furthermore, White teaches that one option to use models in which the lithography process flow 600 is defined to include not only the lithography process step but may also include pre and post photoresist deposition and subsequent plasma etch. [0140]. Additionally, White teaches that the predicted feature dimension variation 680 and the desired feature dimension specification and tolerances 750 are input into a verification and correction component 800 which identifies any features that will exceed or approach the tolerances. [0141].

There is no language in the cited passages that teaches that if a portion of the IC device design is not optimized with respect to process-related variations, then a portion of the IC device design is modified by modifying the density of structures within a portion of the IC device design. Further, there is no language in the cited passages that teaches that if a portion of the IC device design is not optimized with respect to process-related variations, then a portion of the IC device design is modified by modifying the size of a structure with respect to other adjacent structures.

Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 17, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

J. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "wherein the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing" as recited in claim 18, as discussed on pages 17-18 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites paragraphs [0112-0115, 0133, 0140, and 0147-0149] of White as teaching "wherein the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing" as recited in claim 18. Examiner's Answer, page 18. Appellants respectfully traverse.

White instead teaches that lithography is a frequently repeated process step during the manufacture of ICs in which a pattern that defines the dimensions of the circuitry is transferred to a silicon wafer. [0115]. White further teaches that the patterns are subsequently used with the etch process to physically etch the features into the wafer surface or other thin films deposited on the wafer surface. [0115]. White additionally teaches that process related pattern-dependencies may also occur within the lithography process itself where the density of features often affect how well the printed features reproduce those designed. [0133]. Furthermore, White teaches that one option to use models in which the lithography process flow 600 is defined to include not only the lithography process step but may also include pre and post photoresist deposition and subsequent plasma etch. [0140]. Additionally, White teaches that the differences between the two approaches is that in mode A, the design is modified before mask creation and tape-out to produce the desired dimensions and thus the original design and extraction reflect the actual printed circuit dimensions. [0147].

There is no language in the cited passage that teaches that the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 18, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

K. Response to Examiner's assertion that Examiner has provided appropriate motivation for modifying White with Rosenbluth to include the missing claim limitations of claims 10-11, as discussed on pages 18-21 of Examiner's Answer.

As understood by Appellants, the Examiner's new motivation for modifying White with Rosenbluth to have the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity and to have a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations) is "to show that values are indicative of process related variations...improving the design and manufacture of integrated circuits." Examiner's Answer, page 20. The Examiner's new motivation appears to be in part restating the missing claim limitations. The missing claim limitations recite in part "indicative of process-related variations." Hence, the Examiner's new motivation appears to have been gleaned only from Appellants' disclosure (missing claim limitations). Any judgment on obviousness must not include knowledge gleaned only from Appellants' disclosure. *In re McLaughlin*, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 10-11 and 19. M.P.E.P. §2145.

Furthermore, the Examiner states "improving the design and manufacture of integrated circuits" in connection with a motivation for modifying White to include the above-cited missing claim limitations. The Examiner must provide articulated reasoning with some rational underpinning to support the legal conclusion of

obviousness. *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007). The Examiner has not provided any rational underpinning as to how this statement ("improving the design and manufacture of integrated circuits") provides a reason for modifying White to specifically have the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity and to have a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations). There are many ways of improving the design and manufacture of integrated circuits. Why in particular would White be modified to have the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity and to have a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations)? How does this aid the invention in White? Why would one of ordinary skill be motivated to modify White in such a manner?

Hence, the Examiner's motivation does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify White to include the missing claim limitations of claims 10-11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10-11 and 19. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Further, the Examiner now cites paragraphs [0002, 0015, 0019, 0082 and 0099] of Rosenbluth[1] as support for another motivation ("to ensure that integrated circuits are manufactured properly") provided by the Examiner to modify White to include the above-cited missing claim limitations. Examiner's Answer, page 21.

[1] Examiner had previously cited paragraph [0021] of Rosenbluth as support for the Examiner's motivation.

Rosenbluth teaches that many methods have been developed to compensate for the image degradation that occurs when the resolution of optical lithography systems approaches the critical dimensions (CD's) of desired lithographic patterns. [0002]. Rosenbluth further teaches that "phase-shifting chrome" or "attenuated phase shift" improves image sharpness by augmenting the rate of change in illumination amplitude across the edge of mask features. [0015]. Rosenbluth additionally teaches that the optimization in step 0 can be performed against the finite difference between adjacent dark and bright points across feature edges. [0099].

There is no language in Rosenbluth (and in particular cites passages [0002, 0015, 0019, 0082 and 0099]) that makes any suggestion that the feature indicative of process-related variation be at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity or that a larger slope of edge intensity or logarithm of slope of edge intensity be indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity be indicative of a larger process-related variation (missing claim limitations) to ensure that integrated circuits are manufactured properly. The Examiner's source of the Examiner's new motivation (paragraphs [0002, 0015, 0019, 0082 and 0099] of Rosenbluth) does not provide reasons as to why one skilled in the art would modify White to include the missing claim limitations of claims 10-11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10-11 and 19. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

L. Response to Examiner's assertion that White and Hatsch, taken in combination, teach "providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 19, as discussed on pages 22-23 of Examiner's Answer.

In addition to the passages cited by the Examiner in the Final Office Action, the Examiner further cites elements 2660, 2699, 2800, 2810, 2822 and Figures 52A,

52B, 55, 56 and 57 of White as teaching "providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures" as recited in claim 19. Examiner's Answer, page 23. Appellants respectfully traverse.

White instead teaches that in cases, where the system cannot find any corrections to the layout that achieves the design specifications, the design group is notified of the design failure 2660. [0291]. White further teaches that in cases where the system cannot find any corrections to the layout that achieves the design specifications, the design group is notified of the design failure 2699. [0293]. Furthermore, White teaches that an IC design of one or more levels is loaded 2800 and key pattern dependent parameters may be extracted. [0300]. Additionally, White teaches that a comparison is performed 2810 and those sites or IC features that exceed the specified tolerances and the associated variation 2814 and 2816 are used to make corrections within the design or manufacturing processes. [0300]. Further, White teaches that the variation may be used as feedback to facilitate changes in the design process through use of a dummy fill component 2818 where the size and placement of dummy fill is determined and the design modified 2822. [0301].

There is no language in the cited passages that teaches providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 19, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

M. Other matters raised by the Examiner.

All other matters raised by the Examiner have been adequately addressed above and in Appellants' Appeal Brief and therefore will not be addressed herein for the sake of brevity.

II. CONCLUSION:

For the reasons stated above and in Appellants' Appeal Brief, Appellants respectfully assert that the rejections of claims 1-4, 6-20 and 31 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-4, 6-20 and 31.

Respectfully submitted,

WINSTEAD P.C.

Attorneys for Appellants

By: _____
Robert A. Voigt, Jr.
Reg. No. 47,159

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2832

Austin_1 498344v.1